Title: TEST CIRCUIT FOR MEMORY
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DOCKET NO.: 070639-0143

FIG. 1

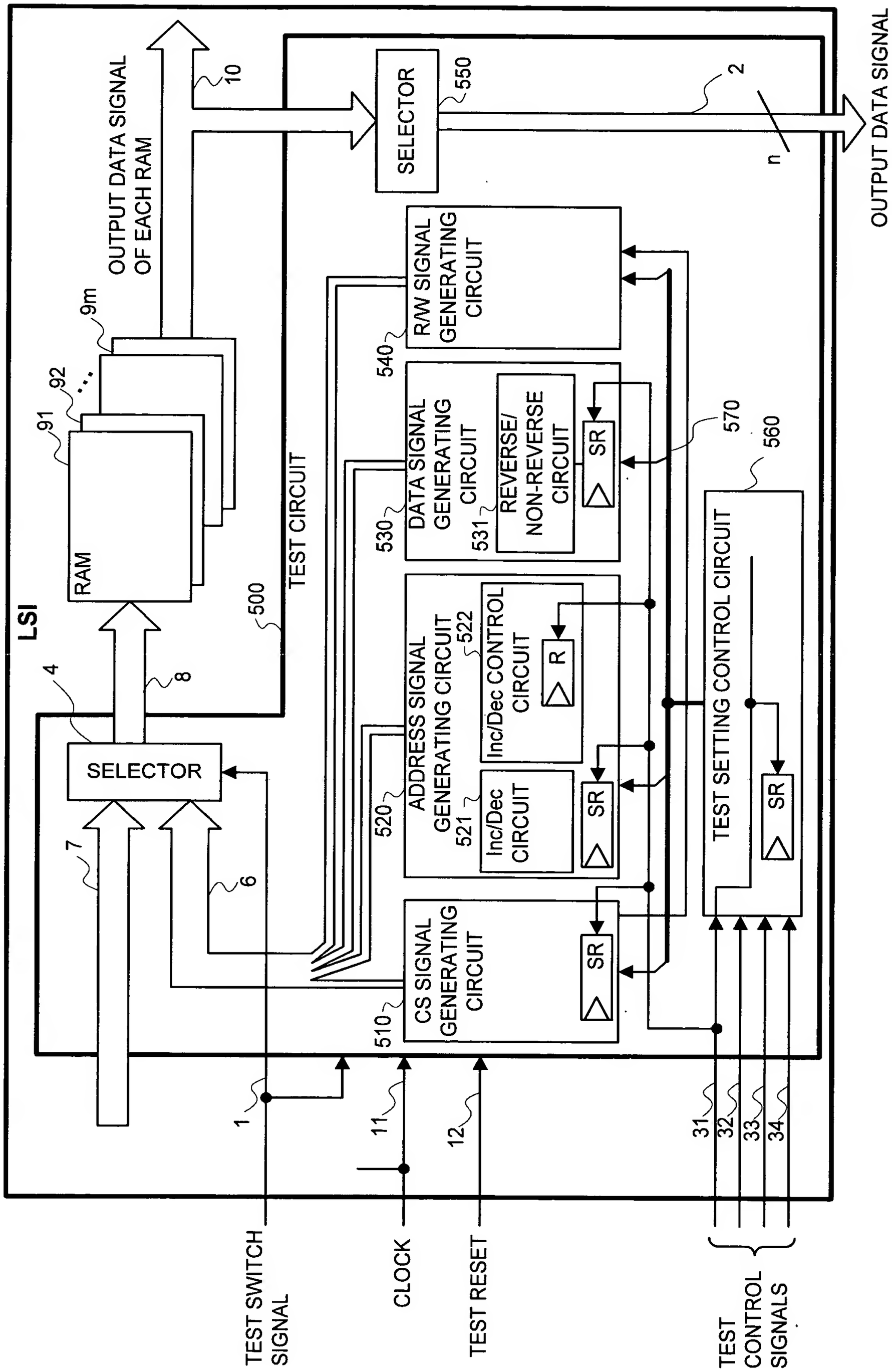

FIG. 2

CONTROL SIGNAL				OPERATION MODE	OPERATION CONTENTS
34	33	32	31		
0	0	0	0	TEST SETTING	NO OPERATION
	0	0	1		RESERVED
	0	1	x		SHIFT SR OF SIGNAL GENERATING CIRCUITS 510-530 AND Inc/Dec CONTROL CIRCUIT 522. INPUT IS CONTROL SIGNAL 31.
	1	0	x		SHIFT SR OF TEST SETTING CONTROL CIRCUIT 560. INPUT IS CONTROL SIGNAL 31.
	1	1	x		RESERVED
1	0/1	x	x	TEST EXECUTION	CONTROL OF PRESENCE OR ABSENCE OF ADDRESS Inc(Dec). 1: PRESENCE 0: ABSENCE
	x	0/1	x		CONTROL OF R/W. 1: W(WRITE) 0: R(READ)
	x	x	0/1		CONTROL OF PRESENCE OR ABSENCE OF DATA REVERSE. 1: REVERSE 0: NON-REVERSE

FIG. 3

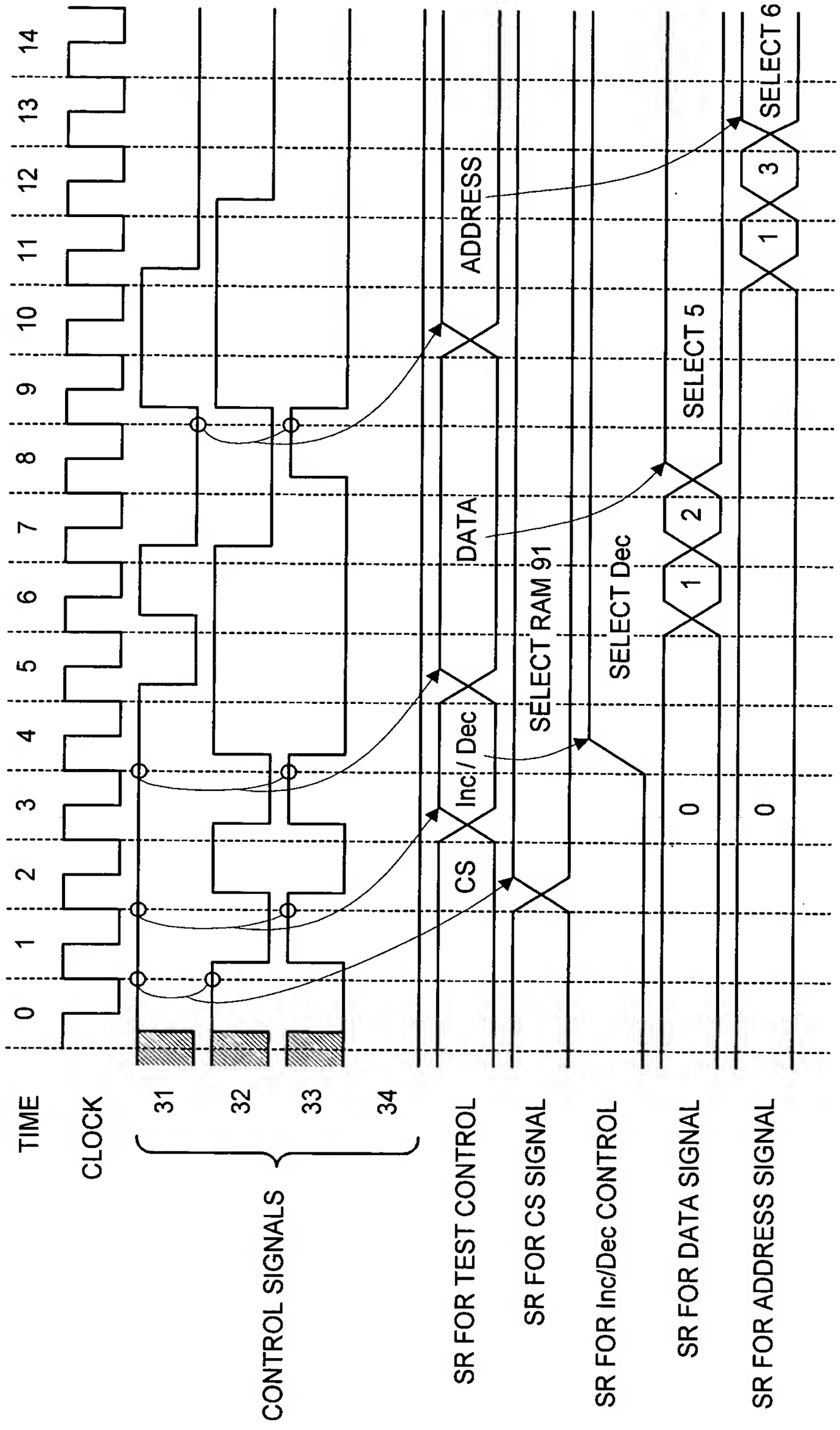
TIME
CLOCK
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
CONTROL SIGNALS
31
32
33
34
SR FOR TEST CONTROL
SR FOR CS SIGNAL
SR FOR Inc/Dec CONTROL
SR FOR DATA SIGNAL
SR FOR ADDRESS SIGNAL
CS
Inc./ Dec
DATA
ADDRESS
SELECT RAM 91
SELECT Dec
SELECT 6
SELECT 5
3
1
2
1
0
0

FIG. 4

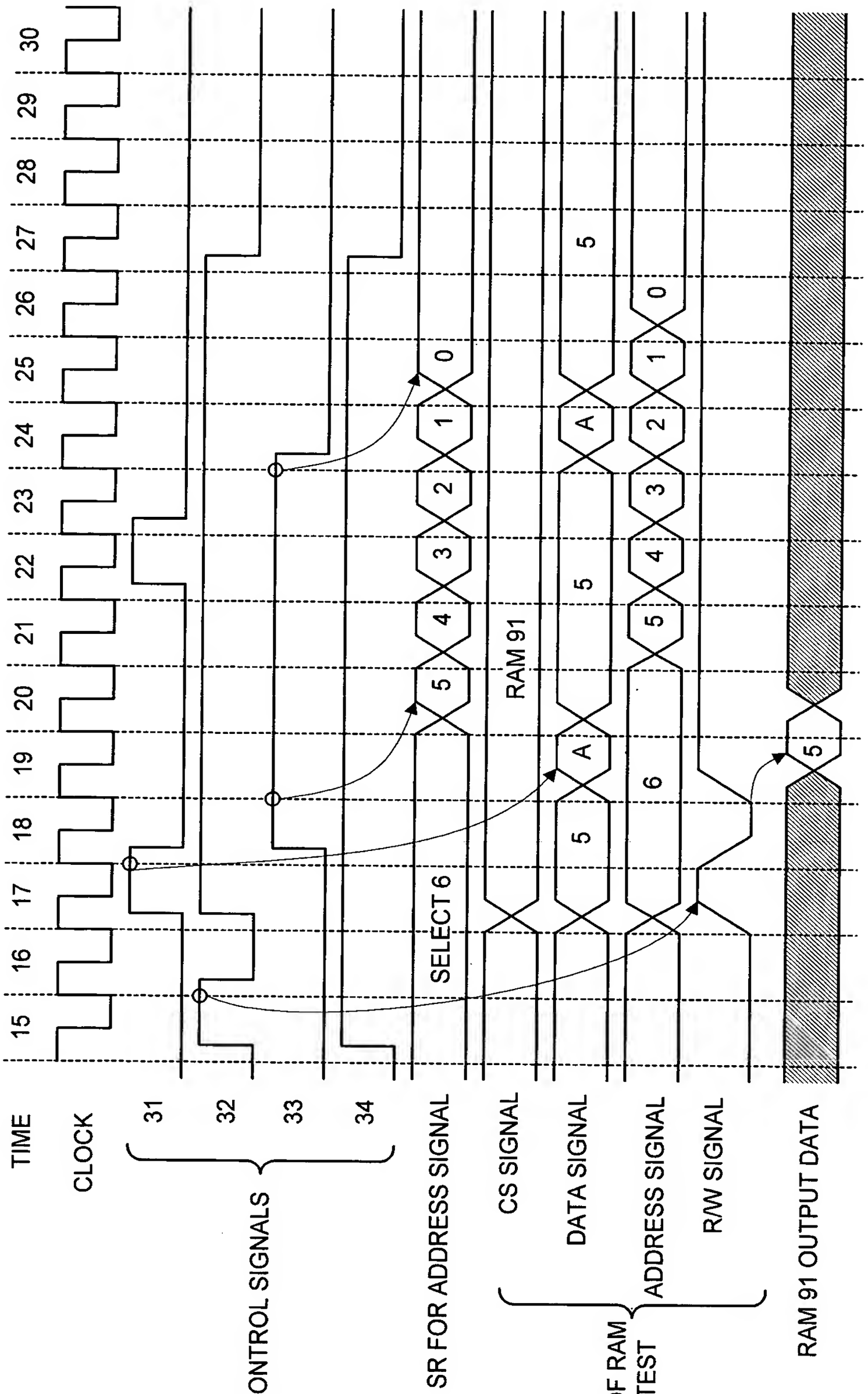
TIME
CLOCK
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
CONTROL SIGNALS
31
32
33
34
SR FOR ADDRESS SIGNAL
SELECT 6
RAM 91
SIGNALS OF RAM DURING TEST
CS SIGNAL
DATA SIGNAL
ADDRESS SIGNAL
R/W SIGNAL
RAM 91 OUTPUT DATA

FIG. 5

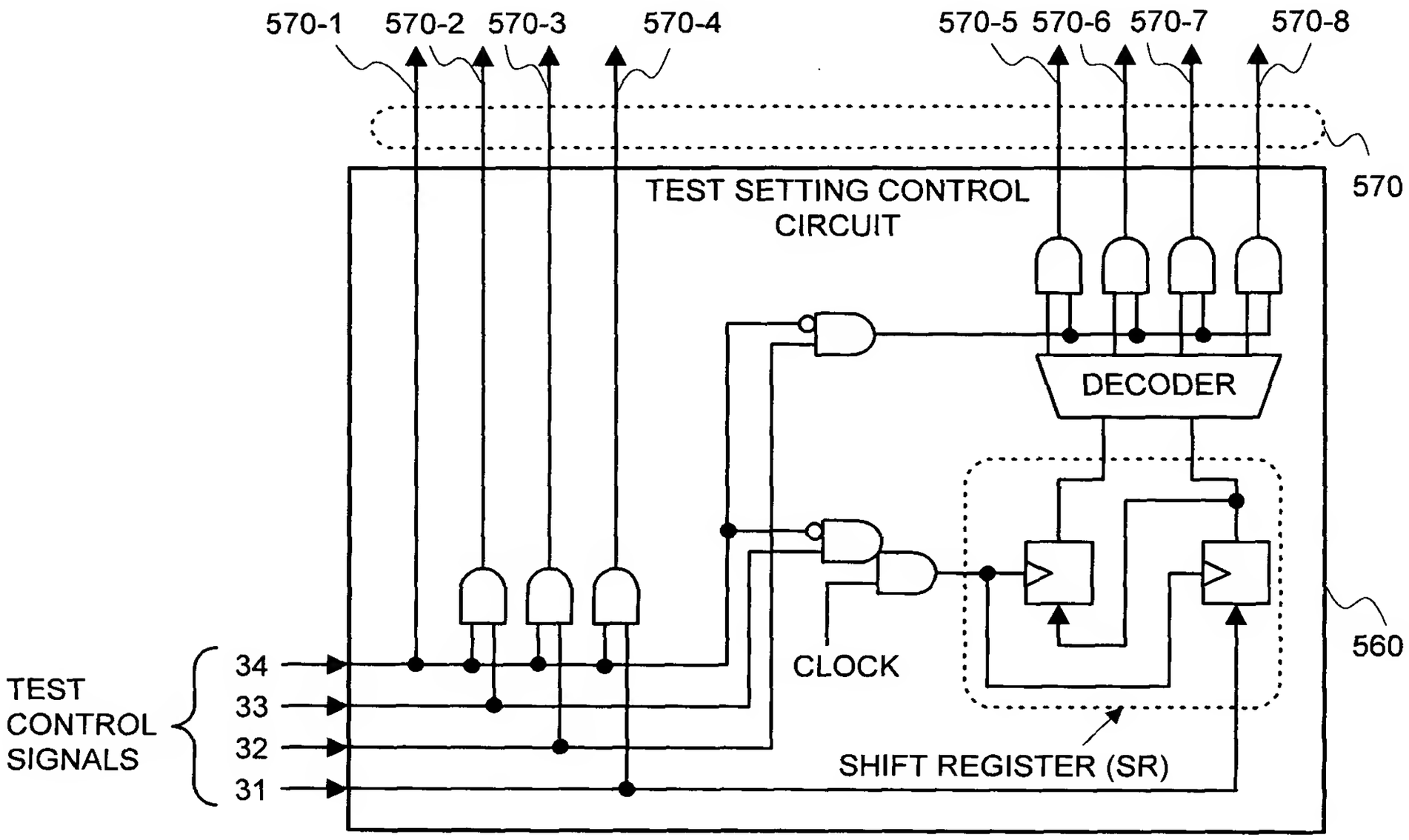
570-1
570-2
570-3
570-4
570-5
570-6
570-7
570-8
570
TEST SETTING CONTROL CIRCUIT
DECODER
CLOCK
560
SHIFT REGISTER (SR)
TEST CONTROL SIGNALS
34
33
32
31

FIG. 6

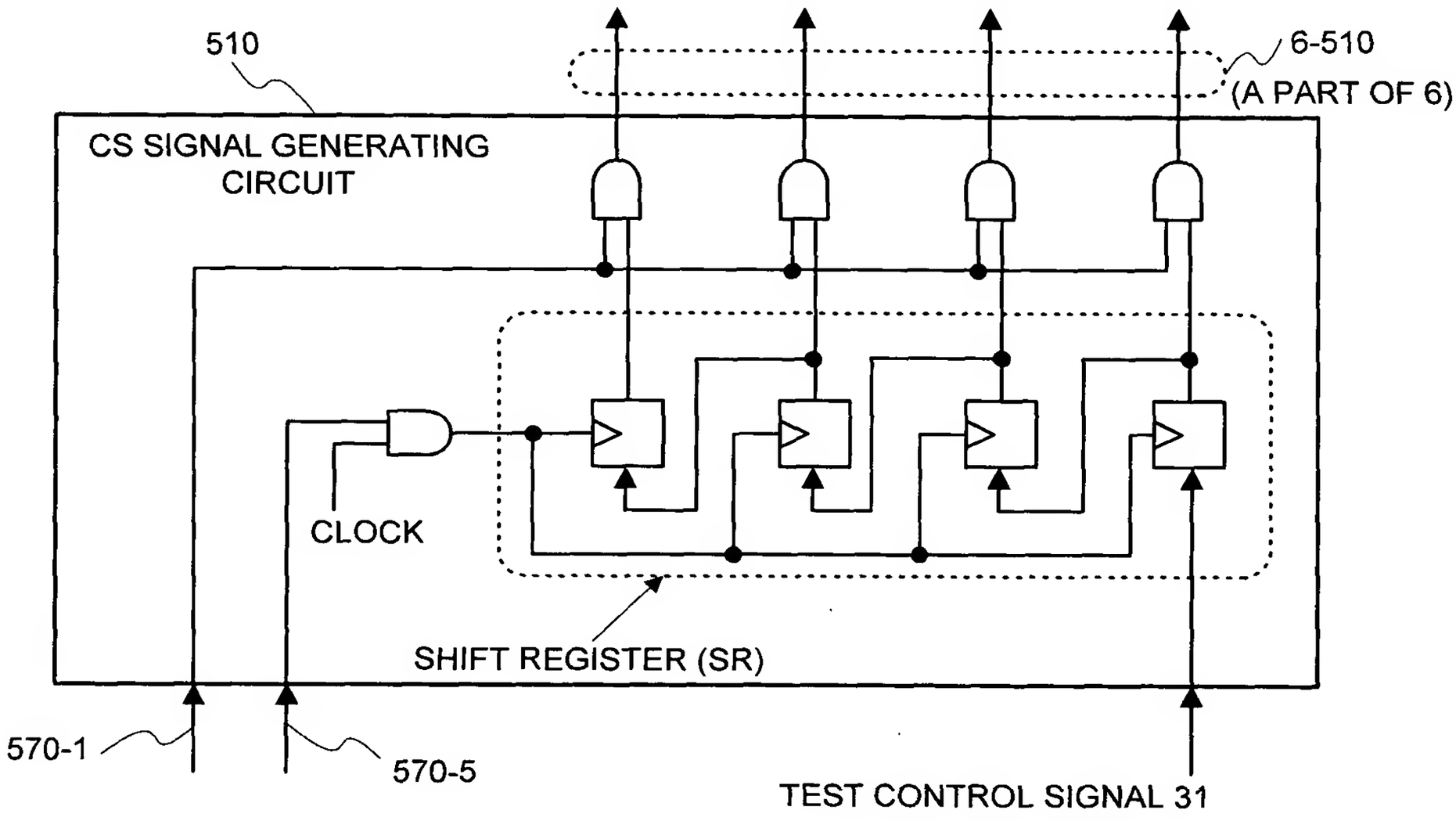
510
6-510
(A PART OF 6)
CS SIGNAL GENERATING CIRCUIT
CLOCK
SHIFT REGISTER (SR)
570-1
570-5
TEST CONTROL SIGNAL 31

FIG. 7

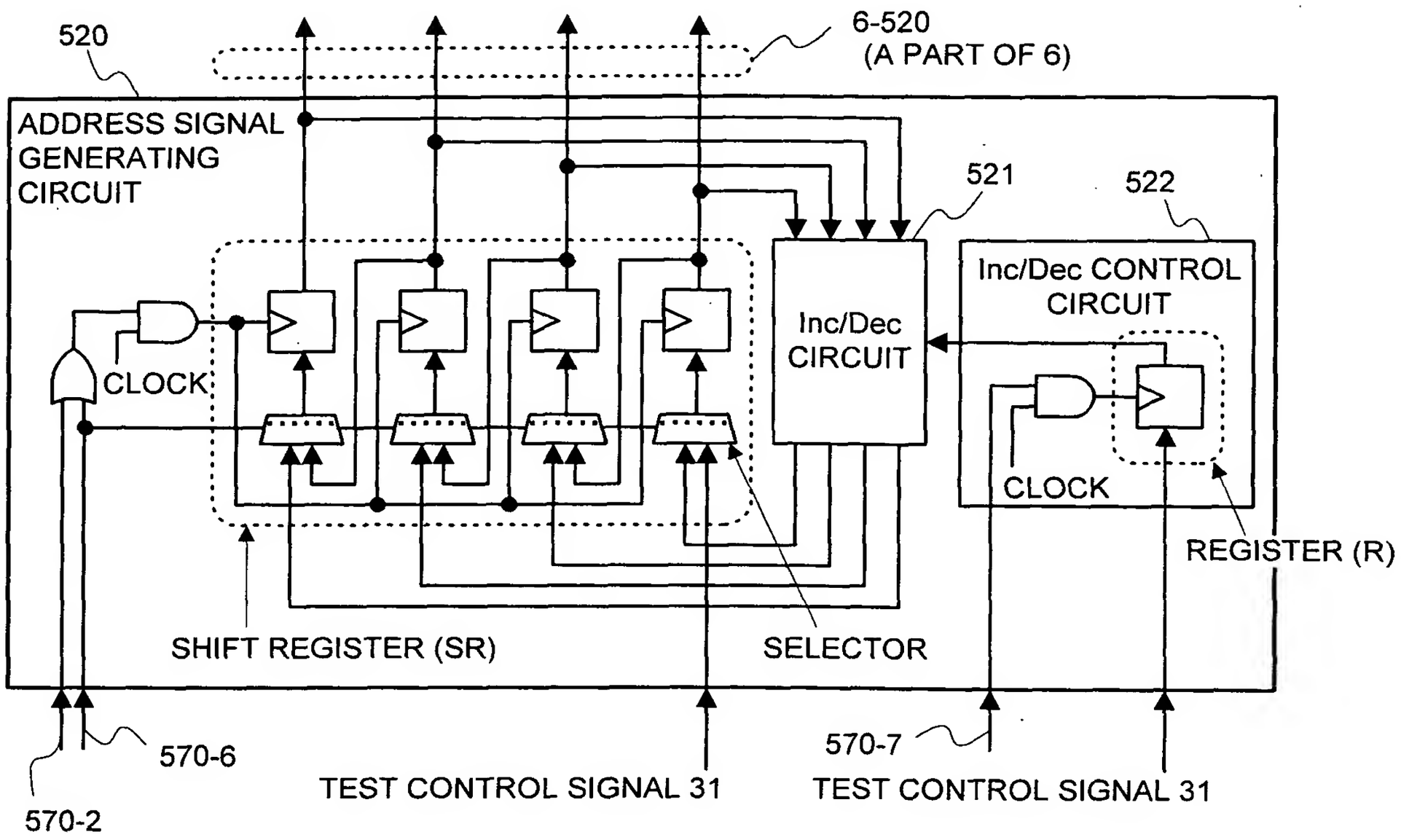
520
6-520
(A PART OF 6)
ADDRESS SIGNAL
GENERATING
CIRCUIT
521
522
Inc/Dec
CIRCUIT
Inc/Dec CONTROL
CIRCUIT
CLOCK
CLOCK
REGISTER (R)
SHIFT REGISTER (SR)
SELECTOR
570-6
570-2
TEST CONTROL SIGNAL 31
570-7
TEST CONTROL SIGNAL 31

FIG. 8

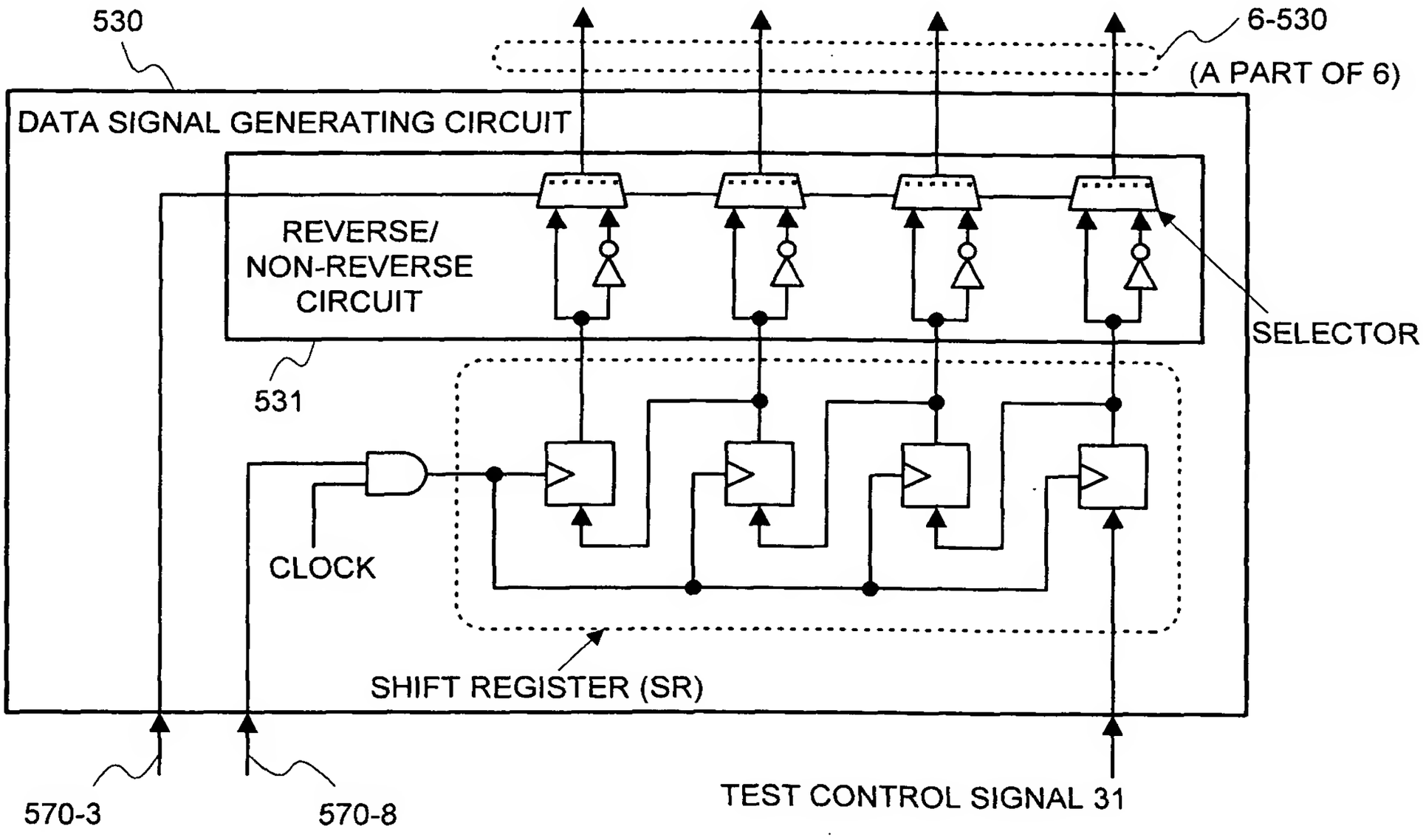
530
6-530
(A PART OF 6)
DATA SIGNAL GENERATING CIRCUIT
REVERSE/
NON-REVERSE
CIRCUIT
531
SELECTOR
CLOCK
SHIFT REGISTER (SR)
570-3
570-8
TEST CONTROL SIGNAL 31

FIG. 9

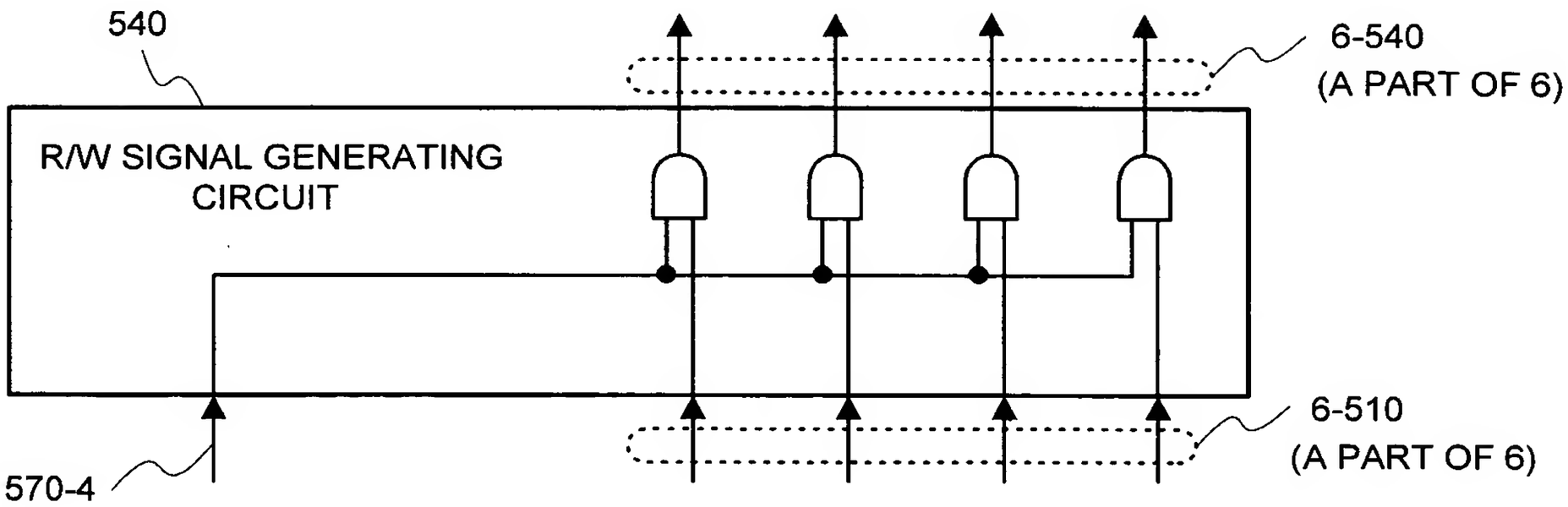

FIG. 10
PRIOR ART

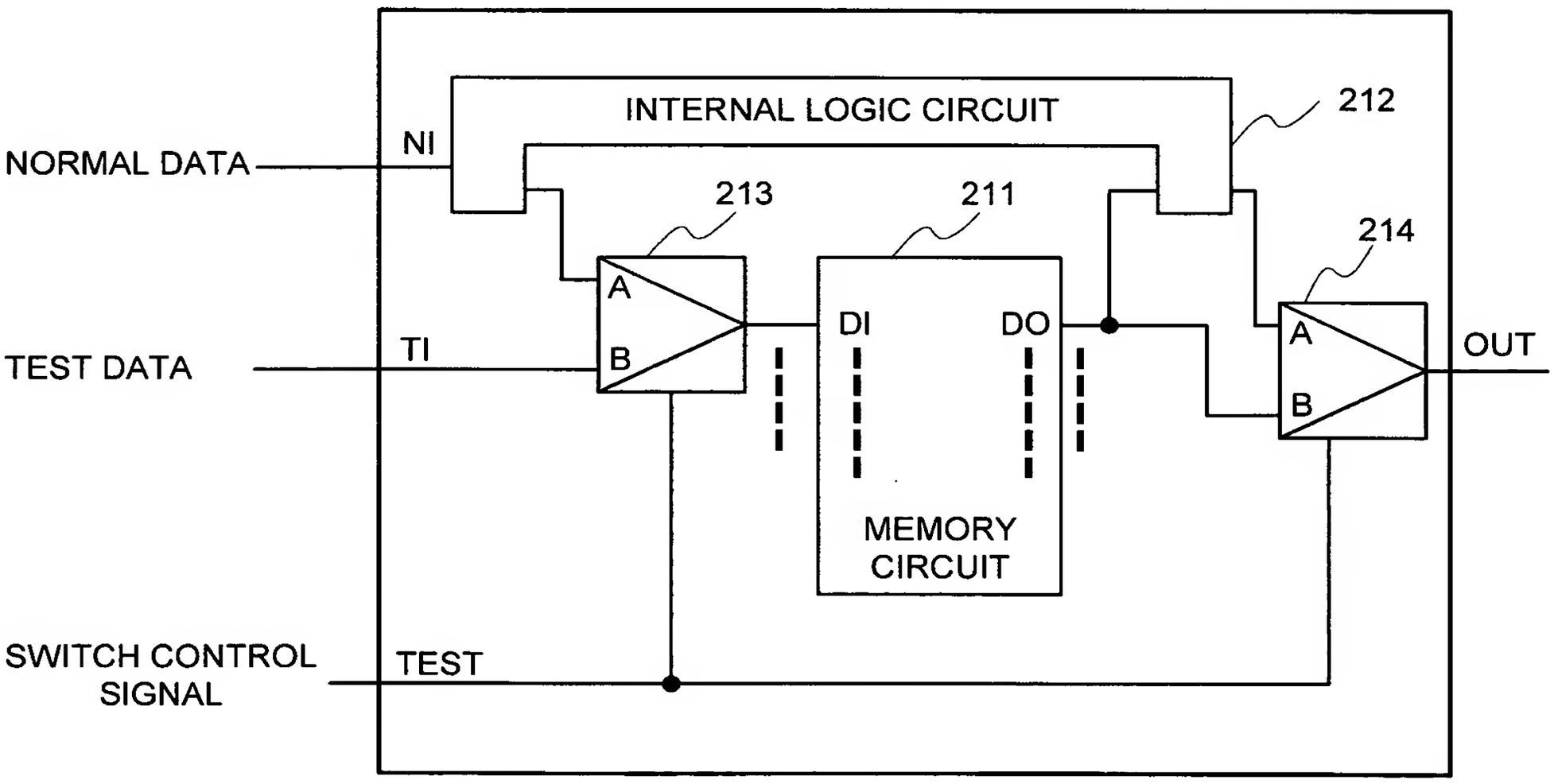
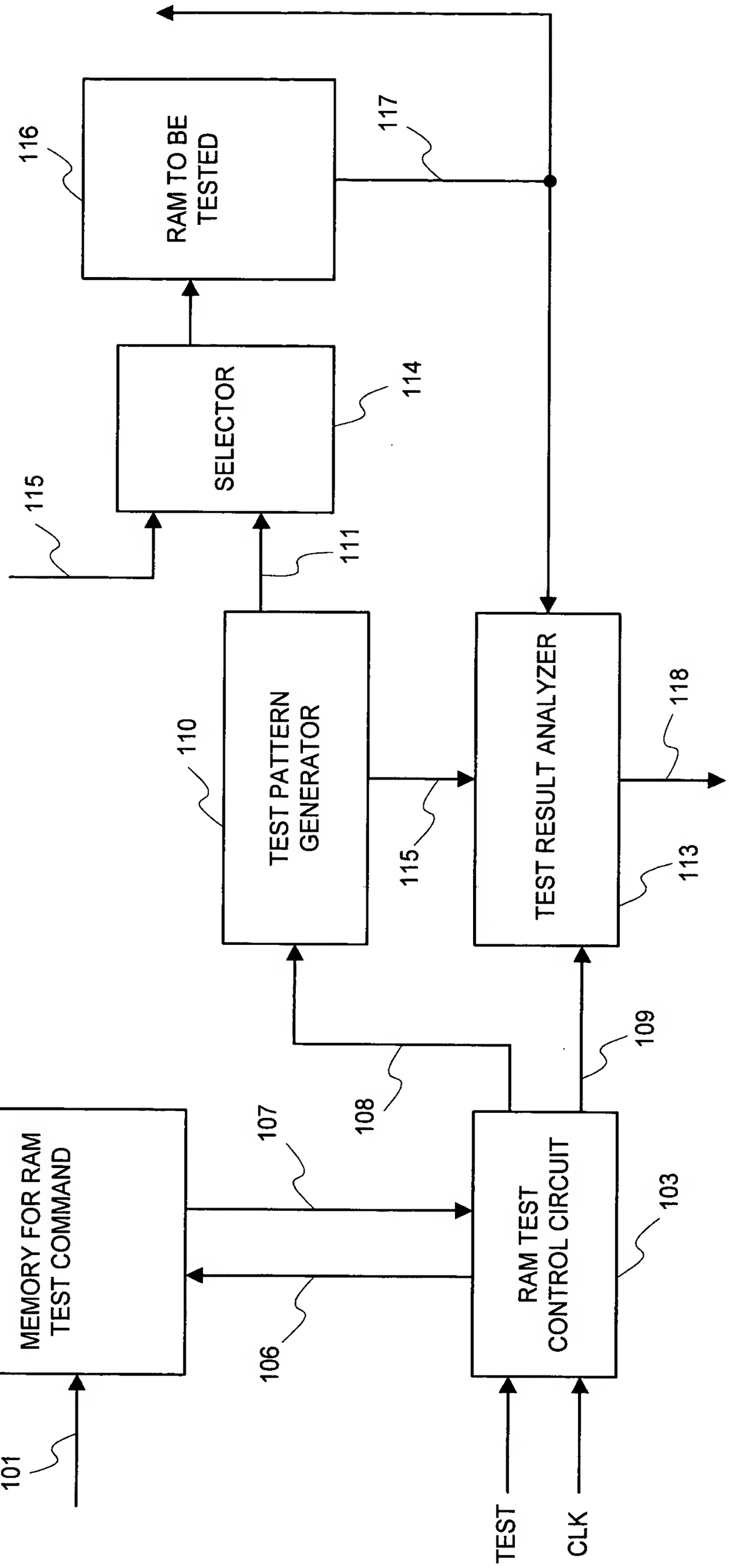
FIG. 11
PRIOR ART